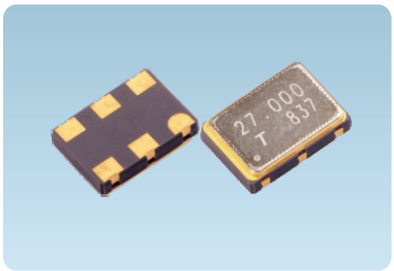
Crystal Oscillator

RoHS compliance

TOT-4 TYPE

Typical 7.0 × 5.0 × 1.75 mm

Very Low phase jitter



Feature

- Typical 7.0 × 5.0 × 1.45 mm 6 pads ceramic SMD package.
- Tight symmetry (45 to 55%) available.
- Ultra low jitter performance: <100fs RMS from 12K~20MHz
- Complementary output.
- High-speed current steering logic (HCSL) output
- Packing:Tape & Reel,1000 pcs per Reel.

Typical Application

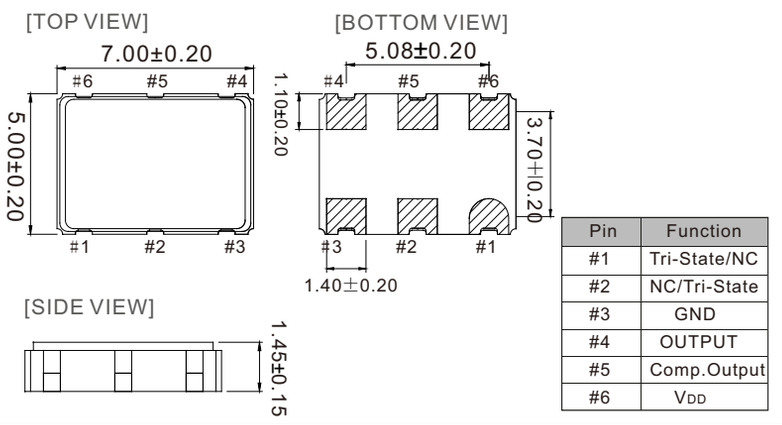
- 40G,100G-BIT,Ethernet,MAN,SONET
- WLAN/WiMax,xDSL,Fiber Channel;Test instrumentation
- PCI-Express

Specifications

Parameter	HCSL				Unit
	3.3V		2.5V		
	Min	Max	Min	Max	
Supply Voltage Variation(VDD)	3.135	3.465	2.375	2.625	V
Frequency Range	25	175	25	175	MHz
Supply Current					
70MHz ≤ Fo ＜ 90MHz	–	–	–	–	mA
90MHz ≤ Fo ＜ 125MHz	–	50	–	50	
125MHz ≤ Fo ≤ 170MHz	–	–	–	–	
Output Level(CMOS)					V
Output High(Logic"1")	–	0.6	–	0.58	
Output Low(Logic"0")	0.15	–	0.15	–	
Transition Time;Rise/Fall Time+	–	0.5	–	0.5	nSec
Start Time	–	3	–	3	mSec
Tri-State(Input to 2 Pin 1)					
Output Activ	0.7V_{DD} Min.				V
Output in High Impedance State	0.3V_{DD} Max.				
RMS Preiod Jitter (Integrrated 12KHz~20MHz)	0.5Max.				PSec
Aging	±3Max.				ppm
Storage Temp. Range	-55~125				°C

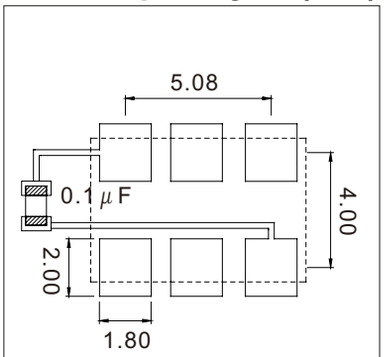
+Transition times are measures between 10% and 90% of VDD,With an output load of 15pF.

Outline Drawing(mm)



Pin	Function
#1	Tri-State/NC
#2	NC/Tri-State
#3	GND
#4	OUTPUT
#5	Comp.Output
#6	V_{DD}

Solder pad layout(mm)



Frequency Stability Vs. Temperature Range

Temp.(℃) \ Ppm	±25	±50
-10 ~ +60	√	√
-20 ~ +70	√	√
-40 ~ +85	+	√

√ Available + Conditional × Not Available

Inclusive of calibration @25℃,operating temperature range, input voltage variation,load variation,aging(1st year), shock,and vibration