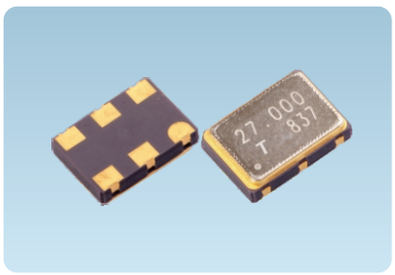
TOT-3 TYPE

Typical 7.0 × 5.0 × 1.75 mm

Highfreq.upto 800MHz



Feature

- Typical 7.0 × 5.0 × 1.75 mm 6 pads ceramic SMD package.
- Tight symmetry(45 to 55%) available.
- High frequency up to 1500MHz.
- Low phase jitter.
- Complementary output.
- Packing:Tape & Reel,1000 pcs per Reel.

Typical Application

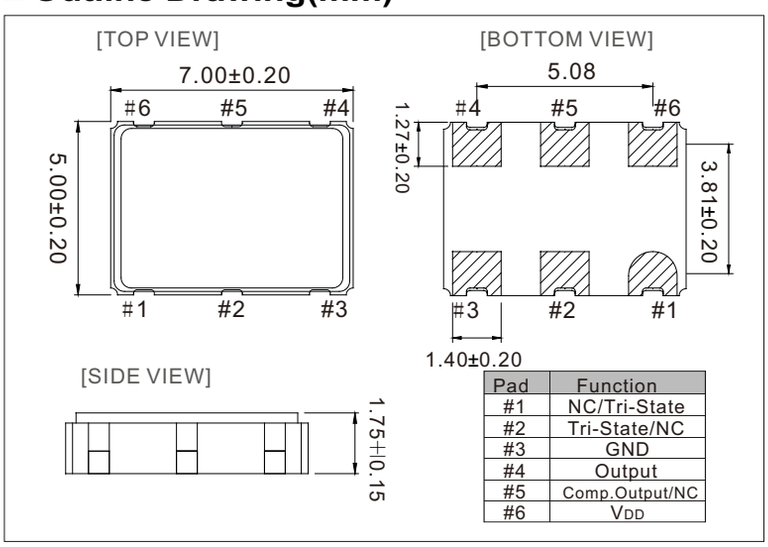
- 10G-BIT,Ethernet,MAN,SONET
- WLAN/WiMax,xDSL
- Fiber Channel

Specifications

Parameter	LVPECL				LVDS				CMOS				Unit
	3.3V		2.5V		3.3V		2.5V		3.3V		2.5V		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Supply Voltage Variation(VDD)	3.135	3.465	2.375	2.625	3.135	3.465	2.375	2.625	3.135	3.465	2.375	2.625	V
Frequency Range	10	1500	10	1500	10	1500	10	1500	10	250	10	250	MHz
Supply Current													
8 Mhz ≤ Fo ≤ 1500 MHz	–	50	–	50	–	50	–	50	–	30	–	30	mA
Output Level(CMOS)													
Output High(Logic"1")	2.275	–	1.475	–	–	1.6	–	1.6	2.97	–	2.25	–	V
Output Low(Logic"0")	–	1.68	–	0.88	0.9	–	0.9	–	–	0.33	–	0.25	
Transition Time;Rise/Fall Time+	–	1.0	–	1.0	–	1.0	–	1.0	–	1.5	–	1.5	nSec
Start Time	–	10	–	10	–	10	–	10	–	10	–	10	mSec
Tri-State(Input to Pin 2 or Pin 1)													
Enable (High voltage or floating)	2.31	–	1.75	–	2.31	–	1.75	–	2.31	–	1.75	–	V
Disable (Low voltage or GND)	–	0.99	–	0.75	–	0.99	–	0.75	–	0.99	–	0.75	
RMS Preiod Jitter (Integrrated 12 KHz~20MHz)	–	1	–	1	–	1	–	1	–	1.0	–	1.0	pSec
Aging (@25℃ 1st year)	–	±3	–	±3	–	±3	–	±3	–	±3	–	±3	ppm
Storage Temp. Range	-55	125	-55	125	-55	125	-55	125	-55	125	125	-55	°C

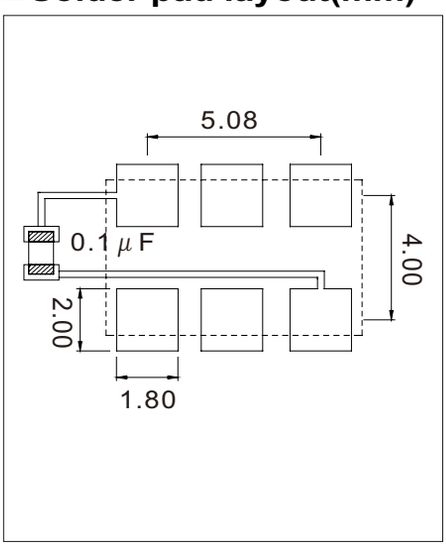
+Transition times are measures between 10% and 90% of VDD,With an output load of 15pF.

Outline Drawing(mm)



Pad	Function
#1	NC/Tri-State
#2	Tri-State/NC
#3	GND
#4	Output
#5	Comp.Output/NC
#6	VDD

Solder pad layout(mm)



Frequency Stability Vs. Temperature Range

Temp.(°C) \ Ppm	±25	±50
-10 ~ +60	✓	✓
-20 ~ +70	✓	✓
-40 ~ +85	+	✓

✓ Available + Conditional × Not Available

Inclusive of calibration @25℃,operating temperature range, input voltage variation,load variation,aging(1st year), shock,and vibration